provided
corresponding to columns. SRAM 200 further includes a row decoder RD connected
to the ends of the plurality of word lines WL, and a column selector CS connected to the ends of the plurality of bit line pairs BL and BL. SRAM 200
further includes a plurality of sense amplifiers SA30 provided corresponding to
the plurality of bit line pairs BL and BL through column selector CS, and a
plurality of bit line loads BR connected to the other ends of the plurality of
bit line pairs BL and BL.

Brief Summary Text - BSTX (8):

Access transistor 52a has its source connected to storage node 54a, its
drain connected to bit line BL, and its gate connected to word line WL. Access
transistor 52b has its source connected to storage node 54b, its drain connected to bit line BL, and its gate connected to word line WL.

Brief Summary Text - BSTX (10):

SRAM 200 operates as follows. In response to an externally applied column
address signal, a column decoder, not shown, drives column selector CS to
connect bit line pair BL and BL and sense amplifier SA30 for a corresponding
column. A constant bias current I.sub.B limited by bit line load BR flows

through each of bit lines BL and BL connected to sense amplifier SA30. In
response to an externally applied row address signal, row decoder RD

FIG. 5 PRIOR ART